

## Autorouting Techniques/Using ELECTRA with Protel

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### Artwork and Autorouting

It is interesting that many engineers and designers believe that high-speed designs still require all manual wiring. Many also believe the "auto" in autorouting is the same functionality as the automatic transmission in a car - simply place the shifter into gear and depress go. Perhaps autorouters should have been named "interactive routers". Then they would perhaps find wider acceptance and would be used correctly more often.

Another common misconception among designers seems to be that autorouting does not create artistic designs, therefore the routing is inferior. After all, it is still artwork, is it not? No. For instance, traces tightly wrapped around each other might create eye-catching patterns, but those tightly-coupled traces may also cause a reset line to trigger, resulting in PCB Rev B. High-speed designs should generally be routed to meet electrical requirements and give less emphasis on eye appeal.

*In this article and tutorial, I will try to cover the steps necessary for preparing a Protel PCB file for autorouting. These steps include:*

- 1. Placement of major components for routability*
- 2. Interactive fanout of SMD components*
- 3. Taking advantage of Protel and 2004 design rules*
- 4. Defining keepouts, using steering graphics, protecting preroutes*
- 5. Pitfalls to avoid*
- 5. Creating route DO files*
- 6. Running the autorouter: Checking progression*
- 7. Retrieving and reviewing route results*

*It is assumed that the reader has sufficient knowledge of the Protel 99SE or 2004 Design platforms.*

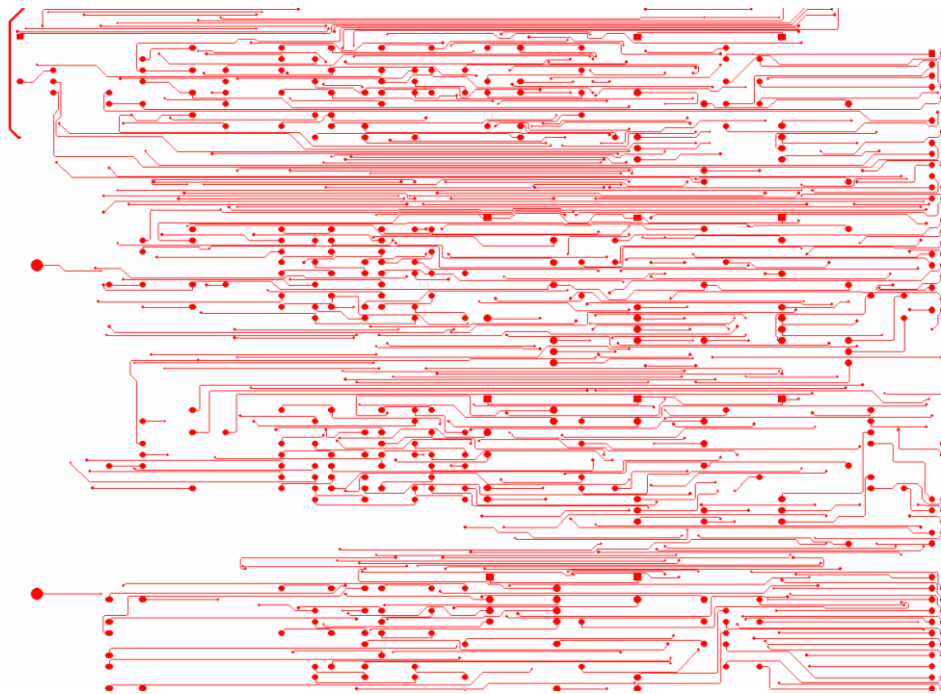
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## Placement and Routing Strategy

Complex multilayer designs require a designer to think about routing strategy early in the design. It is critical to any design that components are placed to meet electrical performance requirements. With large devices such as BGAs and FPGAs, placement has to accommodate power distribution, as well as wiring. Component orientation should be determined by the best wiring solution, not the best artistic or assembly fit.

Correct component orientation is achieved when the rats-nest appears to represent a matrix of horizontal and vertical connections. Straight lines will allow the autorouter to complete connections using the shortest path. The use of this strategy makes it easy to understand why ConnectEDA's ELECTRA autorouter behaves and routes in the same logical manner as we think. If we position components to allow for line of site wiring, the ELECTRA router will achieve efficient, dense routes, normally reaching 100% completion.

A common problem with many designers is not understanding or "thinking" like the router. Designers goals should be to find the shortest path, use the minimal vias and the least number of layers. With high-density designs, the only proven method of achieving these goals is to route traces parallel to each other (reference the route pattern below). Note that these routing patterns may seem contrary to artistic design. However, they are functional and efficient, and are proven with high-speed digital logic.



*Fig. 1 – Clean and straight autorouted internal layer*

Components pads and vias are obstacles to routing, regardless if the routing is performed manually or "automatically". Fewer obstacles exist on the inner layers than on the outer layers. Thus we must look to the internal layers to carry long connections. Internal layers provide the best opportunity for long connections to remain unobstructed. Since all the SMD pads on the outer layers are obstructions, the outer layers serve better for short connections.

As we have divided our connections into short and long traces, it is reasonable to create design rules that would include and exclude nets into outer and inner layer *routes*. You can choose to hand route some of the short nets on the outer layers during the fanout preparation stage.

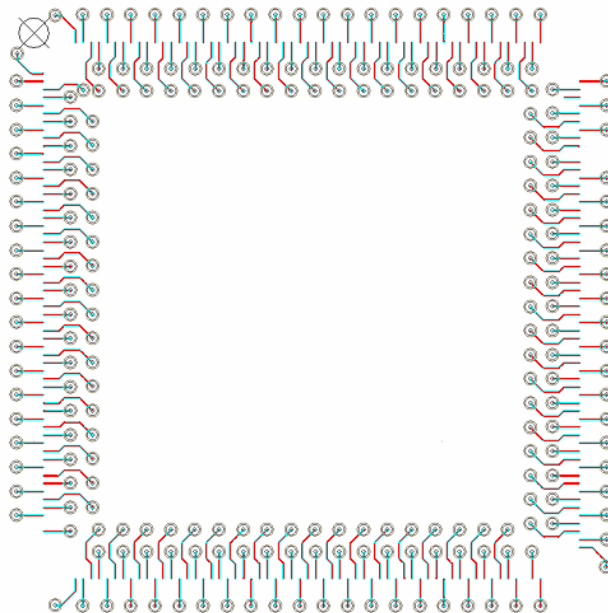
Large components should always be placed first. After the large components are placed, discrete components such as decoupling capacitors and termination resistors can be added to your design.

## **Fan Out and Interactive Wiring**

Second only to the component location, via fanout is the most important preparation task to achieve your routing goals. Careful attention to fanout will determine how quickly and efficiently the router achieves completion. Most often, when the router has not reached 100 percent completion, the problem can be traced to poor fanout. I do not recommend using automatic fanout routines for several reasons.

Performing manual fanout also allows the designer to review, rotate and move discrete components as required. A good fanout has every component pad tied to a via (reference the fanout pattern which follows). Vias should be positioned on grid and must allow for routing channels. A quick method for fanning components is to use pre-fanned components as library parts.

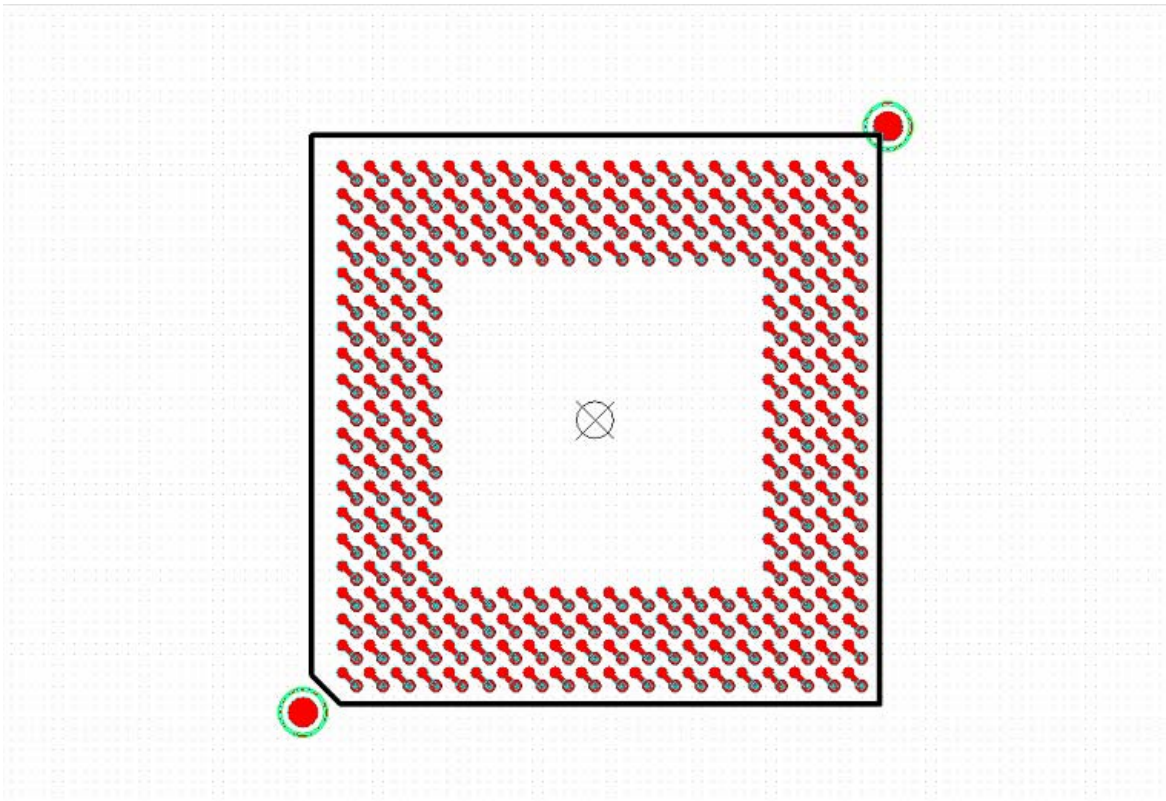
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**Fig. 2 – Pre-fanned QFP library part**

One drawback to this approach is unused pads will contain stubs with a via such as unused pins in a BGA pattern. The extra vias do not pose a manufacturing problem. However, they always remain as an obstacle to the router. My preferred method and more tedious is to create fanout patterns for each size and pitch component.

The fanout libraries should contain patterns for SOICs, QFPs, BGA,s, etc. After a placement review, copy these patterns from your FANOUT.LIB and snap them the footprints pads.



*Fig. 3 – Pre-fanned BGA library part*

After the entire board is fanned-out, globally remove and delete unnecessary pads, traces and vias from unused pads. Depending on the complexity and density of a design, fanout of the large components should take no more than a few hours maximum.

## **Design Rules**

The objective in creating design rules is to translate the routing requirements in to design rules that the router can follow. Few engineers choose to embed routing rules within a schematic, so it is frequently left to the designer to extrapolate the rules. Design rules are not available in the Protel library editors. Therefore create your patterns on a working PCB file using via-to-via clearances, wire-width and trace clearance rules. A via-to-via clearance rule can be added by selecting object kind A, via and object kind B to via. Then set a clearance at  $(2 \times \text{space} + \text{line} + 2 \text{ mils})$ . For example, if the line and space are 5/5, then the total clearance will be 17. The extra two mils guarantees the router will slip traces through easily. If larger clearances are used, then valuable routing channels will be lost. It is important that via-to-via clearances are optimized to allow routes with little real estate loss. On very dense designs, every lost or gained mil becomes critical.

Unfortunately, the Protel DSN file will not contain your via-to-via clearance rule, so the via-to-via clearance must be added separately in either the command line

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or a DO file. The ELECTRA command is: **rule pcb (clearance 17 (type via\_to\_via))**

Copy your patterns to a library for future use. For those that insist on hand routing, I recommend hand routing every discrete component to its connecting pin and fanning pads out manually. The autorouter is capable of connecting discrete components. However, if you design like I do, you might be surprised how many components require tweaking by moving a few mils or 180-degree rotation. Anything gained by last minute optimization will help the router reach maximum completion.

When the fanout is completed, every used pad on every part should have a short connection to a via or discrete components should be routed to their respective pads. If a discrete component requires a connection to the opposite length side of the board, fanout and terminate with a via. This is the best technique to allow the autorouter to easily connect the longer traces.

One question frequently asked by designers is how to prevent vias out of specific areas. One method is to place lines and fills on any unused layers. Keep-out lines between thru hole pads will prevent the router from placing a via between connector pins. Use keep-out fills between discrete component pads to prevent the router from placing vias between SMD pad. This will increase yields during reflow by preventing prevent short circuits between pads. Just make sure that this keep-out layer is OFF and not used for either routing or fabrication purposes. If this layer is not disabled, the router will use it to place traces.

Translate electrical requirements into routing requirements by creating useful and meaningful instructions. One technique is to create and use net classes. Net classes can be included or excluded into routing commands. Assign layers in your layer stack for critical nets or use these layers for controlled impedance wiring.

Assign a net class to specific layers with specific instructions. When a DSN file is exported from PROTEL 2004, the class rules are flattened into individual net instructions. PROTEL 2004 will export the net class name but this action is not functional in PROTEL 99SE. Avoid assigning nets a "priority" number since this does little to instruct the router how to place and route a trace. Another approach is to identify all of the non-critical nets. LEDs, switches, low speed control, even signal requiring large clearances can be assigned to low priority layers in Protel. Typically on a 6-layer design, I might designate two internal layers for critical nets, and two for non-critical nets.

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## Controlled Autorouting

On larger designs, preparation can take several days to a week. Implementing a routing strategy complete with design rules requires time but much less time than manually routing.

There are four methods that can be used for controlled or interactive autorouting:

1. Design rules in Protel
2. Graphics for steering
3. DO files
4. Commands within ELECTRA

Take advantage of the design rules and graphics in Protel to set up your design file since these are the easiest to use. Use keepouts as guides for routing. Routing topologies can be improved on by using routing or steering channels. Use fills and other objects to prevent vias in specified areas. Use design rules to assign specific via sizes to certain nets. Use net classes to set up clearances and trace widths. The design rules will also allow specific routing layers.

There are several rules in addition to via-to-via clearance that do not export well to DSN. These are matched lengths, differential pairs and parallel rules. Most connections will require one layer pair, which will require one via. A good rule is to use max\_via to control the maximum vias allowed by net. The finished results will always be cleaner. For example if a connector has line of sight to a component, and does not require any additional vias, set up design rule for a net class to contain zero vias.

Always make a back up copy of your PCB before importing and exporting to the router. To create a DSN file In DXP/2004, SAVE AS, change the extension to DSN, select all of the export options. Make sure "Protect Preroute" is checked. Do not use the DO file created by PROTEL 2004. Most of your design rules are contained within the PCB file. A relatively small "DO" file can be created using a text editor like WordPad. Another good practice is to review the DSN file in WordPad before loading in the router. Since the PCB file contains most of the rules, my DO files are fairly simple. ELECTRA does an excellent job of protecting nets. Nets are protected by Protel or the command line can be used.

Normally I use the following DO file for routing:

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LIMIT WAY 250
rule pcb (clearance 17 (type via_via)
SELECT ALL WIRES
UNSELECT CLASS ( )
ROUTE 5
FILTER 1
CLEAN 3
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## RECORNER DIAGONAL.

Restricting the routers direction with LIMIT WAY, along with graphic steering and layer assignment will force the router into consistent routing topologies. Consistent topologies yield efficient routes. As a rule, I try routing 97 percent in 5 passes. Import the RTE file from ELECTRA back to Protel. If a trace is not complete, review the routing channels. Estimate how many routed lines are required for your address and data busses, then compare that to how many routing channels are open. If more channels are needed then consider adding layers.

In low-volume designs, adding layers is a cheap compromise. Routes can be reviewed using several methods. A length report is available in both PROTEL 99SE and 2004, or you can toggle through each net using the PCB panel. This allows you to quickly view the topology of each net. A properly routed net should run horizontal and vertical without large loops, or unnecessary stubs and vias. If nets are consistently straying from a short horizontal/vertical routing path, additional layers might be required. After importing a RTE file from ELECTRA, all the vias will contain 28 mil holes. Globally select these vias and change them to their original hole sizes. This is normal behavior seen in several design systems including PADS, Protel and Orcad. The via-to-via design rule should be enabled to locate overlapping vias. Duplicate or overlapping vias can be found on pre-fanned components like BGAs. Globally select these vias from the PCB file, then delete them.

Several passes at the router may be required to get a desired result. Monitor the routing progress. ELECTRA is fast. If the router is stalling out and not making progress, save, then import the RTE file into Protel for review. Slow performance can only be caused by poor layout, insufficient routing layers, conflicts in design rules, or closed routing channels. If these steps are followed, very little or no post clean up is required.

## Pitfalls to Avoid

On rare occasion, a DSN file may not load. All of these problems can be repaired in the PCB file. First, insure the working space with templates, graphics, and text, included does not exceed 50 inches (127 cm) square. This is a fairly large area that should reasonably accommodate almost any design. Insure that all component attributes including reference designators, and comments are also contained within this area. On occasion, a corrupted PCB database will place these attribute outside the Protel workspace. To correct this problem, Select ALL, then Copy everything into a clean PCB sheet, then reload the netlist. The PCB data must also lay in the lower left quadrant of the Protel workspace. The origin can be set either to the workspace or the PC Board outline. Do not use split planes that are not assigned to net.

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There are ongoing debates in manufacturing over the advantages of using round pads versus square pads. Avoid using square pads wherever possible. When a square pad is not assigned to net, on occasion, ELECTRA might place a via over this pad, sometimes requiring minor clean up.

## **Conclusion**

EDA software enhances designers' productivity and it allows them to do more in a shorter space of time, and with a better quality result.

The same is true of autorouters such as ELECTRA. They are a productivity tool that allow PCB designers to perform routing automatically. A proper methodology to implement the use of the autorouter into a PCB design implementation flow provides high productivity gain by shortening the design time and delivers repeatable results.

